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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/526,394	03/16/2000	Wayne J. Howell	BU9-99-175	1550

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EXAMINER	
PAREKH, NITIN	
ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/526,394	Applicant(s) Howell et al
	Examiner Nitin Parekh	Art Unit 2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Oct 17, 2002*.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *2-4, 6, 7, 9-11, 13, 14, and 22-28* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *2-4, 6, 7, 9-11, 13, 14, and 22-28* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 2
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 2, 3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar et al (US Pat. 5290732) in view of Zhao et al (US Pat. 5674787).

Regarding claim 6, Kumar et al disclose a metallurgical/conductive structure in an integrated circuit (IC) chip having underlying circuitry/components within an exterior covering comprising:

- a first layer/line/metal pad (14b in Fig. 9) on the chip/substrate
- a passivation/insulating layer (16b in Fig. 10)
- a via/hole (Fig. 10) through the passivation layer extending to the first layer/metal pad/line
- a barrier layer lining the via (18b in Fig. 10), and

- a metal plug/second layer (40b in Fig. 10) in the via above the barrier layer wherein the metal plug, barrier layer and the passivation layer form a planar exterior surface of the metallurgical structure, the second layer being of predetermined thickness, and
- solder bump/connector/conductive structure (44 in Fig. 10; Col. 6, line 10) comprising conventional lead/tin alloy being in direct contact with the conductive/metal plug (40b in Fig. 10) and the bump being on the planar exterior surface
(Fig. 10; Col. 5, line 23- Col. 6, line 15; Fig. 5-10; Col. 3-12).

Kumar et al disclose the second layer/metal plug/bump being made of material such as copper (Col. 5, line 44) but fails to specify:
a) the metal plug and the line/pad comprising the same material such as copper, and
b) the metal plug having sufficient thickness and forming sufficient intermetallics with elements/species diffusing from the solder bump so as to prevent the elements from penetrating through the barrier layer into or adhering the metal line.

a) Zhao et al teach using the metal plug (23 in Fig. 6) and the metal line comprising conventional material such as copper (Col. 5, line 22; Col. 7, line 25).

The cited reference by Gardner et al teach using an interconnect structure comprising titanium-chromium and copper barrier layers having conventional metal

lines comprising copper, aluminum, etc. and a solder bump for an external connection (Col. 3 and 4).

b) Kumar et al disclose the conductive structure comprising solder ball/bump where the barrier layer/plug comprising conventional adhesion/barrier material such as Ti, TiN, TaN, nickel, etc. with a copper plug of predetermined thickness is used to reduce/prevent the diffusion of elements/species/metals present within the solder bump into the metal line to provide low contact resistance and improved adhesion/reliability (Col. 3, line 36-68; Col. 3-6).

It is well known in chip packaging and interconnection technology art that copper readily reacts and forms intermetallics with elements such as tin from the solder (see admitted prior art- specification page 3, line 12; pages 3 and 4). It would have been obvious to one of ordinary skill in the art to recognize that such layers of copper metal/plug and barrier layer used in Kumar's metallurgical structure would be of sufficient thickness and form sufficient intermetallics with elements diffusing from the solder since the metallurgical structure provides low contact resistance and improved adhesion and reliability.

Furthermore, the determination of parameters such as thickness/number of the barrier layer, plug, diameter/size/number of the solder bump, etc. in chip packaging and

interconnection technology art is a subject of routine experimentation and optimization to achieve the desired adhesion, electrical resistance and reliability.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate elements a) and b) so that the desired electrical resistance, bonding strength and interconnect reliability can be achieved using Zhao et al's material in Kumar et al structure.

Regarding claim 2, the claim elements have been addressed in the rejection as explained above for claim 6.

Regarding claim 3, Kumar et al disclose a barrier layer lining comprising one or more layers of Ti, TiN, Ta and TaN (Col. 3, line 30- Col. 4, line 11) to provide the diffusion barrier between the solder bump metals/species such as tin and the metal pad/line.

3. Claims 4, 7, 9-11, 13, 14 and 22-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar et al (US Pat. 5290732) in view of Zhao et al (US Pat. 5674787) and further in view of Chang et al (US Pat. 5048744) and Havemann (US Pat. 6156651).

Regarding claim 4, as explained above for claim 6, Kumar et al disclose the conductive structure comprising solder ball/bump where the barrier layer/plug comprising conventional adhesion/barrier material such as Ti, TiN, TaN, nickel, etc. with a copper plug of predetermined thickness is used to reduce/prevent the diffusion of elements/species/metals present within the solder bump into the metal line to provide low contact resistance and improved adhesion/reliability (Col. 3, line 36-68).

It is well known in chip packaging and interconnection technology art that copper readily reacts and forms intermetallics with elements such as tin from the solder (see admitted prior art- specification page 3, line 12; pages 3 and 4).

Furthermore, the use of barrier layers such as Ti, TiN, Cr, etc. to provide the diffusion barrier against elements/impurities from solder and to improve adhesion, bond strength and reliability of the interconnection/solder joint is well-known in the chip packaging and interconnection technology art (see prior art disclosed by Gardner et al: Col. 1, line 51). The cited reference by Chang et al teach using Cr/Ti barrier layer to improve the conductivity between the solder and the metal such as copper (Col. 7, line 10; Col. 8, line 33; Fig. 8-11).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a barrier layer and a metal plug to prevent the diffusion of elements within the solder bump into the metal line so that the desired

adhesion, electrical resistance and interconnect reliability can be achieved using Chang et al's teaching in Kumar et al's structure in view of Zhao et al.

Regarding claim 7, Kumar et al fail to specify a second barrier layer above the metal plug and second metal plug above the second barrier layer with the second metal plug being in direct contact with the solder bump.

Havemann teaches using conventional multilevel structure forming two levels of copper plugs/grooves with TiN barrier layer such that the second barrier layer is above the first metal plug and second metal plug is above the second barrier layer (Fig. 3G; Col. 4, line 55- Col. 5, line 38).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a second barrier layer above the metal plug and second metal plug above the second barrier layer with the second metal plug being in direct contact with the solder ball so that the diffusion of elements within the solder bump into the metal line can be prevented and the reliability of the interconnection can be improved using Havemann's teaching in Kumar et al's structure in view of Zhao et al.

Regarding claims 9-11, 13, 14 and 22, the claim elements have been addressed in the rejections as explained above for claims 6, 2-4, 7 and 6 respectively.

Regarding claims 23-28, the claim elements have been addressed in the rejections as explained above for claims 6 and 2-4.

Response to Arguments

5. Applicant's arguments filed on 10-17-02 have been fully considered but they are not persuasive.

A. Applicant contends that Kumar et al disclose using a thin metal plug/layer using a metal cluster ion deposition method and the metal plug/layer is not thick enough to prevent the penetration of the materials from the solder.

However, as explained above, Kumar et al disclose the barrier layer/plug conductive structure having solder bump where the barrier layer comprising a conventional adhesion/barrier material such as Ti, TiN, TaN, nickel, etc. with a copper plug of predetermined thickness is used to provide a function of a barrier to prevent the diffusion of elements/species present within the solder bump into the metal line to provide low contact resistance and improved adhesion/reliability (Col. 3, line 36-68). Furthermore, a material such as copper being highly reactive with elements such as tin from the solder and readily forms intermetallics (see admitted prior art- specification page 3, line 12; pages 3 and 4) so that the composite barrier/plug structure of

predetermined thickness in Kumar et al would obviously provide the desired barrier against the diffusion/penetration of the materials from the solder.

Furthermore, the determination of parameters such as thickness/number of the barrier layer, plug, diameter/size/number of the solder bump, etc. in chip packaging and interconnection technology art is a subject of routine experimentation and optimization to achieve the desired adhesion, electrical resistance and reliability. It would have been obvious to one of ordinary skill in the art to arrive at the optimized thickness to achieve the improved adhesion and to prevent the penetration of the materials from the solder.

B. Applicant contends that Zhao et al does not teach using a solder bump directly above the copper plug.

However, as explained above, Kumar et al discloses the aluminum metal line. Zhao et al teach a structure comprising the metal plug (23 in Fig. 6) made of copper and the metal line being of conventional metals such as copper or aluminum (Col. 5, line 22; Col. 7, line 25). Therefore, Zhao's conventional metal line structure is applied to Kumar et al to achieve the desired electrical performance.

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number in (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

12-17-02

Tom Thomas

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